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AUG 09 2005

Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (previously presented) A shared delay circuit of a semiconductor device comprising:

an input signal conversion unit for converting a plurality of input signals into a plurality of pulse signals;

a delay unit for detecting a predetermined signal level of any one of the plurality of pulse signals and outputting a delayed pulse signal that is formed by a plurality of the detected pulses delayed for a predetermined time ; and

a switch and output control unit for receiving the plurality of pulse signals and the delayed pulse signal delayed for the predetermined time through the delay unit, and outputting a plurality of delayed output signals,

wherein each of the plurality of delayed output signals is in the substantially same signal form as the corresponding one of the plurality of input signals inputted into the input signal conversion unit.

2. (previously presented) The shared delay circuit of claim 1, wherein the input signal conversion unit has a plurality of pulse conversion units, each of which corresponds to each of the plurality of input signals.

3. (previously presented) The shared delay circuit of claim 1, wherein the plurality of input signals are level signals or pulse signals.

4. (previously presented) The shared delay circuit of claim 1, wherein the delay unit comprises:

a pulse signal detection unit for detecting whether any one of the plurality of pulse signals exceeds the predetermined signal level and outputting the detected pulse ; and

a delay control unit for receiving the detected pulse and delaying the detected pulse for a predetermined time, and outputting series of the detected pulses as the delayed pulse signal

5. (previously presented) The shared delay circuit of claim 4, wherein the pulse signal detection unit is a NAND gate or a NOR gate.

6. (previously presented) The shared delay circuit of claim 1,

wherein the switch and output control unit comprises a plurality of switches and output control units which correspond to the plurality of pulse signals; and

wherein the switch and output control units are activated by the plurality of pulse signals and the delayed pulse signal outputted from the delay control unit, and converts the plurality of pulse signals into the plurality of delayed output signals having a delay.

7. (original) The shared delay circuit of claim 1,

wherein the switch and output control unit comprises a plurality of switch and output control units which correspond to the plurality of pulse signals, and each of the switch and output control unit comprises a switch, a switch control unit and a control unit; and

wherein the switch control unit controls an on/off operation of the switch, the switch passes therethrough and applies the delayed pulse signal to the control unit, and the control unit converts the input delayed pulse signal into the input signal form.

8. (original) The shared delay circuit of claim 7, wherein the switch control unit enters into a standby mode by an output signal of the control unit.

9. (original) The shared delay circuit of claim 7, wherein after the output signal is outputted from the control unit, the switch control unit and the control unit compulsorily enter into a standby mode by an external signal.

10-11. **(cancelled)**